Capacitor Design Guidelines:

- MLCC's age due to a phenomenon known as *oxygen vacancy migration.* This phenomenon results in a limited device lifetime accelerated by voltage and temperature stress. X5R and X6S capacitors have a shorter life time, in power applications, due to the lower temperature ratings (85 °C for X5R and 105 °C for X6S). Therefore, it is recommended that capacitor life be estimated using the **Prokopowicz and Vaskas** (PV) equation and manufacturer's HALT data for the specific part at the circuit operating conditions.
- Electrolytic capacitors fail due to excess voltage, reverse voltage and the evaporation of electrolyte (which is a function of the core temperature resultant from the ambient temperature plus the temperature rise due to the square of the ripple current times the ESR of the capacitor).
- The life/endurance calculation **shall** be performed using the equation provided by the specific capacitor manufacturer.
- The breakdown voltage of an electrolytic is not at an abrupt voltage, but rather it is related to the thickness of a chemically generated oxide on the electrodes. If the working voltage slowly increases, the oxide thickness, and therefore the voltage capability of the capacitor, increases. Similarly the reverse is true if the working voltage reduces. The dc voltage + low frequency ac ripple **shall not** exceed the rated DC voltage.
- Aluminum electrolytic types are used for bulk low frequency filtering.
- Care must be taken when placing capacitors, especially electrolytic, in the vicinity of high temperature components.
- Capacitors must have a temperature rating of at least 105 °C. Reducing the operating core temperature is necessary to obtain 10 year life.
- Solid tantalum capacitors **shall not** be used for the following reasons: when failing as a short, they can ignite and burn due to use of MnO_2, the material used in pyrotechnic mixtures, causing serious damage to printed wiring boards and nearby components. Use polymer tantalum or polymer aluminum capacitors instead.
- Polymer capacitors like OsCon, Poscap, Ta polymers and Al polymers are observed to have fewer failures in the field than solid tantalum and electrolytics.
- 0805 and larger size SMD ceramic capacitors can develop cracks during the assembly process. Certain series of ceramic capacitors from some manufacturers contain a safety margin in their internal plate construction. Capacitor designs with a safety-designed part do develop cracks but these cracks usually do not lead to shorting.
- CLASS II and CLASS III dielectric SMT MLCC capacitors, 1206 or larger, rated 50V or 100V and used across a DC telecom power bus **shall** be "Fail-Open" (or equivalent) type. The use of SMT MLCC capacitors larger than 1210 **shall** require customer's approval.
- Z5U and Y5V types are not recommended due to higher temperature coefficient, lower temperature range and weak structure.
- SMD ceramic capacitors **shall not** be located on the PWB in areas that are subject to board flexing such as along the edge of a board or in a location where mating of connectors, mating of test fixtures, or transportation induced vibration causes board flexing.
- SMD ceramic capacitors of sizes larger than 1210 should only be used when special precautions are taken to mitigate the risk of cracking (such as capacitors with polymer terminations).
- Variable capacitors are not to be used as they are unreliable.

Table A-2 Derating Guidelines for Resistors

Device Type	Parameter	Class II Stress Factor[1]	Class I Stress Factor[1]
Resistors			
Fixed Film (Discrete and SMD Thin-Film, Thick-Film and Metal Oxide)	Power Dissipation	≤60%	≤70%
	Peak Pulse Power	Below Supplier Rating	Below Supplier Rating
	Maximum Working Voltage	≤70%	≤70%
	Below Maximum Temperature Limit	≥25 °C	≥25 °C
	SMD Maximum Body Temperature	100 °C	≤100 °C
Zero Ohm	Current	≤85%	≤85%
Carbon Composition	Power Dissipation	≤60%	≤70%
	Maximum Working Voltage	≤60%	Below Supplier Rating
	Below Maximum Temperature Limit	≥25 °C	≥25 °C
Wirewound Power	Power Dissipation	≤70%	≤70%
	Maximum Working Voltage	≤60%	Below Supplier Rating
	Below Maximum Temperature Limit	≥6 °C	≥6 °C
Variable	Power Dissipation	≤40%	≤70%
	Maximum Working Voltage	≤50%	≤50%
	Wirewound Below Maximum Temperature Limit	≥20 °C	≥20 °C
	Nonwirewound Below Maximum Temperature Limit	≥30 °C	≥30 °C
Thermistor	Power Dissipation	≤50%	≤50%
	Maximum Working Voltage	≤80%	Below Supplier Rating
	Below Maximum Temperature Limit	≥20 °C	≥20 °C
Metal Oxide Varistors	Power Dissipation	≤60%	≤60%
	Operating Voltage/Clamping Voltage	≤30%	≤30%
	Maximum Current	≤90%	≤90%
	Rated RMS Voltage	≤90%	≤90%
	Maximum Energy for All Timings	≤90%	≤90%
Thick Film Network	Power Dissipation	≤70%	≤70%
	Below Maximum Temperature Limit	≥24 °C	≥24 °C
	SMD Maximum Body Temperature	≤100 °C	Below Supplier Rating

1. Stress Factor is the applied level divided by rating: a 12 volt rated part used at 9 volts has a 75% stress factor.

Resistor Design Guidelines:

- Failures in resistors are caused by excessive power dissipation, high ambient temperature, or excessive joules in pulsed in applications.
- All film resistors and to a lesser extent other types of resistors have a limited capability to handle high peak power pulses even though the average power dissipation may be within rating. Refer to the manufacturer's data sheet for peak powers versus time and duty cycle. If high pulse powers are expected, a solid element composition, ceramic-carbon or wire wound resistor may be more appropriate.
- Leaded film resistors are trimmed to their final value by cutting a helix in the film. High value resistors used in line voltage, 400V bus and snubber applications are subject to a number of reliability issues. These resistors have a high spiral turns count that leads to a very narrow element width and hot-spot problems. The laser cut is very narrow leading to high voltage field levels and ionization between turns.
- Chip film resistors are trimmed by making a cut or series of cuts across the resistor. Excessive trimming will lead to narrow sections that will develop into hot spots.
- Metal film resistors are recommended over carbon types. Since carbon is less stable over humidity and life, they are not recommended where drift may be an issue.
- Wire wound resistors are recommended for dissipation greater than 2 Watts, for stability and reliability reasons.
- Potentiometers are to be avoided, if possible, due to the need for adjustability in manufacturing and low reliability. Where two terminals of the potentiometer are normally connected for potentiometer operation, the variation effect could be made small and may not affect reliability. Device ratings are to be met for low or zero resistance adjustment.
- Considerations **shall** be given to low inductance resistor types whenever necessary.
- Follow the guidelines for resistor mounting to be properly spaced from the PCB surface.
- The maximum stress on any resistor due to line transients, safety testing etc., **shall not** exceed the manufacturer's 'Maximum Overload Voltage' or equivalent specification.
- Thermistors used for surge limiting have a specific capability to absorb a single power pulse when charging large bulk capacitors, particularly in off line power supplies. The rating may be in the form of maximum capacitance.
- Varistors are used for shunt regulators and for transient protection:
  - Shunt regulator: working voltage is limited by power dissipation.
  - Transient protection: working voltage is limited by power dissipation over the normal voltage range and by Energy or Amps-Seconds for transients.
- Beware of SMD thick film resistor construction in regard to the method of inner layer nickel deposition and the silver termination. The dipped type methods are inferior to the plated methods. The dipped types allow gaps that will expose inner silver substrates to atmospheric sulphur compounds which can lead to corrosion and long term failures (opens). In addition, the silver plating should be doped with palladium to retard the silver sulfide crystal growth. It is recommended that thick film resistors of an anti-sulfuration design be used in potted applications.

Table A-3 Derating Guidelines for Diodes and Transistors

Device Type	Parameter	Classes I and II Stress Factors[1,2]
Diodes		
General Purpose (Signal or Switching - Junction, PiN, Schottky)	Forward Current	≤90%
	Reverse Voltage	≤70%
	Power	≤75%
	Maximum T_j	≤T_j maximum - 25 °C
Power Rectifier (Schottky and Non-Schottky)	Average Forward Current	≤90%
	Reverse Voltage	≤80% / ≤80% including repetitive spikes; a single event spike at 90% of maximum rating.
	Maximum T_j	≤T_j maximum - 25 °C
	Power	≤70%
Silicon Carbide Power Rectifier Do Not Avalanche SiC Diodes	Forward Current	≤80%
	Reverse Voltage	≤80%
	Maximum T_j	≤T_j maximum - 25 °C
Transient Voltage Suppressor	Peak Power	≤70%
	Peak Forward Surge Current	≤70%
	Maximum T_j	≤T_j maximum - 25 °C
Voltage Regulator/Reference (including Zener)	Power Dissipation	≤50%
	Maximum T_j	≤T_j maximum - 25 °C
Thyristor, SCR and Triac	Transient Energy	≤80%
	On-State Current (It)	≤90%
	Off-State Voltage (Vr)	≤70%
	Maximum T_j	≤T_j maximum - 25 °C
Microwave	Power	≤90%
	Reverse Voltage	≤70%
	Maximum T_j	≤T_j maximum - 25 °C
LED GaAs GaP GaN-SiC GaAsP AlGaAs	Power	≤70%
	Forward Current	≤70%
	Reverse Voltage Peak	≤80%
	Maximum T_j	≤T_j maximum - 25 °C
Photo Diode	Power Dissipation	≤80%
	Current	≤75%
	Voltage	≤75%
	Maximum T_j	≤T_j maximum - 25 °C
Injection Laser Diode	Power Output	≤75%
	Maximum T_j	≤T_j maximum - 25 °C
Transistors		
Silicon Bipolar - Small Signal or Power	Power	≤75%
	Collector-Emitter Voltage	≤80%
	Emitter-Base Voltage	≤80%
	Collector Current	≤60%
	Maximum Junction Temperature (T_j)	≤T_j maximum - 25 °C
Silicon FET - Small Signal	Drain - Source Breakdown Voltage	≤80%
	Gate - Source Voltage	≤80%
	Drain Current	≤80%
	Maximum Junction Temperature (T_j)	≤T_j maximum - 25 °C
	ESD Rating	>1000V
	Power PD	≤75%

Device Type	Parameter	Classes I and II Stress Factors[1,2]
Power MOSFET and IGBT	Drain Current/Collector Current	≤90%/≤90% including peak current
	Drain - Source/Collector - Emitter Voltage	≤90%/≤90% including repetitive spikes for devices rated <200V; energy in single event spikes must not exceed 50% of avalanche rating. ≤80%/≤80% including repetitive spikes for devices rated >200V; single event spike at 95% of maximum rating.
	Gate - Source Voltage	≤80%
	Maximum Junction Temperature (T_j)	≤T_j maximum - 25 °C
	dv/dt Rating	5V/nsec max. if reverse recovering the body diode. 30V/nsec - 40V/nsec in capacitive charging applications.
	Power Dissipation	≤80%
Photo Transistor	Current	≤75%
	Voltage	≤75%
	Maximum T_j	≤T_j maximum - 25 °C
FET GaAs	Power Dissipation	≤90%
	Maximum Channel Temperature	≤T_j maximum - 25 °C
Hetro Junction Bipolar GaAs	Power Dissipation	≤90%
	Maximum Channel Temperature	≤T_j maximum - 25 °C
High Mobility GaAs	Power Dissipation	≤90%
	Maximum Channel Temperature	≤T_j maximum - 25 °C

1. Stress Factor is the applied level divided by rating: a 12 volt rated part used at 9 volts has a 75% stress factor.
2. Semiconductor devices do not wear out like many other component types under normal operating conditions, therefore only one stress level is defined.

Diode Design Guidelines:

- In bridge rectifiers, typical failures are due to excessive surge current and reverse voltage conditions. In universal power supplies, a minimum of 600 Volts Peak-Inverse-Voltage is recommended for the diodes.
- Switching losses and conduction losses contribute to the total power dissipation for diodes in switching circuits. When determining the rating, the PIV of the diodes at high temperatures of operation **shall** be taken into account.
- Extreme precaution needs to be taken for assembly of diodes into a heat sink. Insulation and torque of the screws need to be properly specified to avoid any failures of the diodes.
- If diodes are in series, then, to share the break down voltage, a resistor and a capacitor **shall** be used in parallel to each diode. The maximum junction temperature for this particular case **shall** be reduced to 100 °C. If diodes (rectifiers) are in parallel, it is recommended that the devices share the same heatsink to balance the Vf. This does not apply to dual die parts where the derating is provided in the part specification.
- The power dissipation in a Schottky rectifier will come from RMS current losses + average current losses + leakage current losses. There are significant components of each.
- Excessive power dissipation is the primary reason for failure of the zener diodes.
- A series resistor **shall** be used to limit the current (power dissipation) through the zener.
- A capacitor across the zener stabilizes the zener voltage and reduces high frequency noise.
- Zeners that have a voltage rating close to 5V have the lowest temperature coefficient for the voltage.
- Biasing the zeners at the manufacturer's test level of current provides an accurate value for the zener voltage in circuit.

Transistor Design Guidelines:

- The main causes of failure in transistors are elevated junction temperatures and voltages exceeding the rated breakdown voltage of the device. The measured voltage **shall** include all transient conditions (dynamic loading or starting conditions).
- MOSFETS in parallel require Gate circuit inductance and gate resistance of the PCB layout to be matched as much as possible in order to avoid oscillation and subsequent gate oxide failure.
- Usage of TO220 devices is to be avoided whenever possible. The leads must have insulating sleeves and an insulation coating **shall** be applied at the intersection of the leads and the body of the device and also where the leads intersect the PCB. This applies to 'high' voltage applications where arcing and catastrophic failure is a real possibility due to zinc and tin whisker and other metallic contamination.
- For transistors, the supplier **shall** allow for the degradation of parameters over time:
  - Gain (± 50%).
  - Leakage Current - I_{CBO} or I_{CEO} (+100%).
  - Switching times (± 20%).
  - Saturation Voltage (± 20%).
- The supplier **shall** use base to emitter resistors to reduce false turn on due to leakage.
- Extreme precaution needs to be taken for assembly of semiconductors into a heat sink. Insulation and torquing for the screws need to be properly specified to avoid any failures of the semiconductors. Gap fillers should be used where appropriate. Gang type mounting should be scrutinized to avoid unequal mounting forces.
- Static electricity can damage or destroy a MOSFET, especially gate to source voltages. Handling and design **shall** minimize the possibility of ESD events on the gate.
- To prevent oscillations, the supplier **shall** use gate resistors when FETS are paralleled. The resistor provides damping to dampen the ringing due to parasitic inductance and gate capacitances.
- MOSFET device **shall not** be avalanched on any repetitive basis, and possibility of avalanching **shall** be minimized even during worst-case (such as start-up or shut-down) or fault conditions.
- Be wary of power ratings - they are usually specified at a case temperature of 25 °C. Apply the appropriate derating curve for higher case/ambient temperatures (provided by supplier).

Table A-4 Derating Guidelines for Magnetics

Device Type	Parameter	Class II Stress Factor[1]	Class I Stress Factor[1]
Magnetics			
Power Inductors	Maximum Hot Spot Temperature (Below Insulation Rating) [2]	≤25 °C	≤25 °C
Power - Transformers	Maximum Hot Spot Temperature (Below Insulation Rating) [2]	≤25 °C	≤25 °C
	Temperature below specified Fuse Temperature - This applies to transformer designs with fuse operation required to meet safety compliance.	≤15 °C	≤15 °C
EMI Filter Coils	Power	≤80%	≤80%
	Current dc	≤90%	≤90%
	Voltage Surge	≤90%	≤90%
	Maximum Hot Spot Temperature (Below Insulation Rating) [2]	≤25 °C	≤25 °C
Powdered Iron Core (Including: dc Chokes) Note: Designs utilizing powdered iron cores must use proper thermal derating to prevent thermal aging, which can lead to overheated insulation on transformer wires that may result in fire.	Maximum Core Temperature and/or Hot Spot Temperature	≤100 °C	≤100 °C

1. Stress Factor is the applied level divided by rating: a 12 volt rated part used at 9 volts has a 75% stress factor.
2. Insulation Ratings: Class A - 105 °C Class B - 130 °C Class F - 155 °C Class H - 180 °C.
3. Transformers **shall** comply to IEC 60950-1 and IEC 60664-1 safety standards.

Magnetics Design Guidelines:

- In general, for linear operation, the flux density of operation **shall** be far below the saturation flux density of the device core. The flux density of operation is a design limit which is highly dependent on the temperature characteristics of the specific core used. For example, 4500 Gauss (450mT) at 10 Oersteds (800A/M) may be the core specification saturation flux density but a practical design limit might be 2850 Gauss at 2 Oersteds. Given the saturation flux density roll off at 100 °C, the usable flux density may be from 2600 Gauss to 3200 Gauss.
- Exceeding the rated hot spot temperature of the insulation will reduce the life of a device.
- Structural parts of a magnetics assembly **shall not** be operated at temperatures above the temperature rating of the materials used.
- Adhesives used in SMD or other magnetic parts should be evaluated at maximum hot and cold temperatures to ensure there is no "cold flow" or cracking resulting in loose construction and gap changes.
- Winding specifications should include tension monitoring to prevent wire stretching and insulation cracking.
- Temperature Guidelines and Selection are dependent of Processing Temperature Profiles, and Heat Exposures. The total time at temperature above Operational Temperature needs to be taken into consideration when selecting wire, adhesives, and insulation materials.
- All Cores have a Curie Temperature at which point the Core no longer exhibits Magnetic Properties.
- Material Reliability is related to a Flux Density Operation Level and a Specific Temperature Point at which the Loss is Stable and no increasing thermal destabilization or thermal runaway condition is present.
- Thermal Aging of Magnetic Materials is based on Breakdown of the Organic Binders Present (Powdered Iron Cores).
- Core Selection Guidelines or Parameters are Circuit Design Dependent in determining the Maximum Operating Temperature for Material Performance and Reliability.

Transformers:

- Power transformer operation at low frequencies may result in overheating, due to lower reactance allowing large currents.
- Some power transformers generate large magnetic fields, which can couple ac signals into nearby circuits. Use appropriately shielded transformers, separate shielding and adequate spacing where needed.
- Transformers have been identified to have potential for influencing Electromagnetic characteristics of system. Change in component type **shall** be reviewed for EMC impact.

Inductors:

- Ensure that power inductor core binder material does not contain stearic acid, octadecanoic acid, hexadecanoic acid or other long-chain acids that may break down over time. Use of such materials with internal spot temperatures over 130 °C can lead to rapid failure after a short-to-moderate time of apparently normal operation.
- Be careful that dc current does not saturate the magnetic core, which will drastically change inductor characteristics.
- SMT inductors and filters are susceptible to damage by soldering heat. Keep temperature ramp less than 4 °C/second by gradual preheating, to avoid cracking of the internal layers.
- SMD or through-hole components with large numbers of ferrite layers are most susceptible to thermal shock and impact stresses.
- Open circuits can occur due to mechanical damage to component body or body-termination bond from vibration, shock or overload during service life; and from flexure, vibration or shock during assembly.
- Through-hole inductors may fail due to weakening of internal low temperature solder connections by assembly soldering heat. Welded internal connections avoid this risk.
- Provide conductive heat transfer paths and locate inductors for best cooling.
- Make sure that circuits driving inductive loads are characterized for their Safe Operating Area or employ appropriate transient suppression.
- Inductors have been identified to have potential for influencing Electromagnetic characteristics of system. Change in component type **shall** be reviewed for EMC impact.

Table A-5 Derating Guidelines for Microcircuits and Hybrid Microcircuits

Device Type	Parameter	Class II Stress Factor[1]	Class I Stress Factor[1]
Microcircuits			
Silicon Digital (MOS and Bipolar)	Output Current	≤80%	Below Supplier Rating
	Frequency	≤90%	Below Supplier Rating
	Maximum Junction Temperature **shall** be below maximum supplier's rating	≤T_j maximum - 25 °C	≤T_j maximum - 25 °C
Silicon Linear ICs (Bipolar)	Input Voltage	≤85%	Below Supplier Rating
	Output Voltage[2]	≤80%	≤80%
	Output Current	≤80%	≤90%
	Maximum Junction Temperature **shall** be below maximum supplier's rating	≤T_j maximum - 25 °C	≤T_j maximum - 25 °C
Silicon Linear ICs (JFET and MOS)	Input Voltage	≤70%	Below Supplier Rating
	Output Voltage[2]	≤80%	≤80%
	Output Current	≤90%	≤90%
	Maximum Junction Temperature **shall** be below maximum supplier's rating	≤T_j maximum- 25 °C	≤T_j maximum - 25 °C
Hybrid Microcircuits			
Thick Film Resistor	Power Dissipation	≤70%	≤70%
Thin Film Resistor	Power Dissipation	≤70%	≤70%
Chip Resistor	Power Dissipation	≤70%	≤70%
Chip Capacitor	Voltage	≤70%	≤70%
Gen Purpose Diode	Forward Current	≤90%	≤90%
	Reverse Voltage	≤80%	≤80%
Microwave Diode	Power Dissipation	≤90%	≤90%
	Reverse Voltage	≤80%	≤80%
Bipolar Transistor	Power Dissipation	≤90%	≤90%
	Voltage (Vce)	≤80%	≤80%
FET	Power Dissipation	≤90%	≤90%
	Breakdown Voltage	≤90%	≤90%
Hybrid Package	Maximum T_j	≤T_j maximum - 25 °C	≤T_j maximum - 25 °C

1. Stress Factor is the applied level divided by rating: a 12 volt rated part used at 9 volts has a 75% stress factor.
2. Output voltage derating does not apply to fixed voltage regulator integrated circuits.

Monolithic and Hybrid Microcircuit Design Guidelines:

- Continuous Power needs to be derated such that any tolerance or errors in design, other components, or operating conditions never bring the actual power above the maximum recommended operating power given by the device specifications or Datasheet.
- Maximum Core Voltage needs to be derated such that any tolerance or errors in design, other components, or operating conditions never bring the actual Core Voltage above the maximum recommended operating Core Voltage.
- Minimum Core Voltage needs to be Derated such that any Tolerance or errors in design, other components, or operating conditions never bring the actual Core Voltage below the minimum recommended operating Core Voltage.
- Maximum IO Voltage needs to be derated such that any tolerance or errors in design, other components, or operating conditions never bring the actual IO Voltage above the maximum recommended operating IO Voltage.
- Minimum IO Voltage needs to be derated such that any tolerance or errors in design, other components, or operating conditions never bring the actual IO Voltage below the minimum recommended operating IO Voltage.
- Maximum Operating Frequency needs to be derated to below the specified Maximum Operating Frequency toallow for device performance degradation over time due to Hot Carrier Injection (HCI) and Negative Bias Transistor Instability (NBTI) effects. HCI and NBTI effects degrade MPU performance by causing core transistor VT to drift upwards with the passage of time; (absolute value of VT for PMOS transistors). This especially affects processors and DRAMs.

- Be aware of minimum operating frequency problems. Do not operate dynamic circuits below the minimum specified clock frequency; or they will "forget" data, particularly at high temperatures!
- The Turn-on sequence (of input signals, output loads, clocks and PCD voltages) is often crucial. The wrong Turn-on sequence (such as input voltages higher than or present before supply voltages) can result in latch-up, with permanent damage to the IC. Input clamping diodes to supply and ground may be necessary at interfaces between separately powered circuits.
- *Follow IC manufacturer's recommendations for terminating unused inputs; in general, they* ***shall not*** *be left floating.* To minimize component count, several inputs may be terminated by the same resistor(s).
- Linear ICs, both bipolar and MOS, are generally very susceptible to ESD damage. *Sub-catastrophic ESD* damage can increase noise and shift DC operating parameters, and lead to erratic operation and functional failure over time.
- The slew rate of a linear circuit may be limited by available current so that full scale output is not possible over its full bandwidth. For example, an amplifier may have a small signal bandwidth of 1 MHz and be capable of an output of 20 volts peak to peak, but to do both at once without distortion requires a slew rate capability of more than 63 volts/µsec.
- Linear ICs usually have parasitic thermal feedback. For example, the zero offset of the input stage of an operational amplifier or comparator will change as the output changes amplitude or polarity, because temperature changes of the output stage affect the input state on the same die. Thermally induced offset shifts, of 50 µV to 1 mV (referred to input) are common, unless the IC layout has been designed to minimize this effect.

Table A-6 Derating Guidelines for Miscellaneous Electricals and Electronics

Device Type	Parameter	Class II Stress Factor[1]	Class I Stress Factor[1]
Miscellaneous			
Circuit Breakers (Note 2)	Current	≤60%	≤80%
	Voltage	≤60%	Below Supplier Rating
Fuses (Metal Element)	Current (Normal Blow)	≤90%	≤90%
	Current (Time Delay - Slow Blow)	≤85%	≤85%
	I^2t Rating	≤70%	≤70%
Fuses (Resetable Poly-Element Fuses) Note these Degrade over Time	Operating Current/$I_{Holding}$	≤50%	≤80%
	Fault Current/I_{Max}	≤50%	≤80%
	Voltage	≤70%	≤80%
Fans - See IPC-9591 Performance Parameters for Air Moving Devices	RPM Average	90% of Maximum	100% of Maximum
	Bearing Load	See Supplier Specs	See Supplier Specs
	Temperature Below Maximum Ambient Limit	≥10 °C	≥5 °C
Connectors (Circular/PWB/Coaxial) (Connectors - Power) (Connectors, Relays and Switches with oxidizing contacts)	Voltage	≤70%	≤70%
	Current	≤70%	≤70%
	Insert Temperature below Maximum Limit	≥25 °C	≥25 °C
	For Primary Voltages	Note 2	Note 2
	Minimum Dry Circuit Voltage	≥12V	≥12V
	Minimum Dry Circuit Current	≥100mA	≥100mA
Relays	Resistive Load Current	≤75%	≤75%
	Capacitive Load Current	≤75%	≤75%
	Inductive Load Current (Nonclamped)	≤40%	≤40%
	Inductive Load Current (Clamped)	≤75%	≤75%
	Motor Load Current	≤20%	≤20%
	Filament (Lamp) Current	≤10%	≤10%
	Contact Voltage (ac or dc)	≤50%	Below Supplier Rating
	Contact Power	≤50%	≤50%
	Drive Voltage Minimum/Rated Minimum	≥110%	Below Supplier Rating
	Drive Voltage Maximum/Rated Maximum	100% Maximum	Below Supplier Rating
	Temperature Below Maximum Limit	≥20 °C	Below Supplier Rating

Device Type	Parameter	Class II Stress Factor[1]	Class I Stress Factor[1]
Miscellaneous			
Switches (General Purpose)	Contact Current - Resistive Load	≤75%	≤90%
	Contact Current - Capacitive Load	≤75%	≤90%
	Contact Current - Inductive Load	≤40%	≤75%
	Inductive Load Current (Clamped)	≤75%	≤75%
	Contact Current - Motor Load	≤20%	≤30%
	Contact Current - Filament (Lamp) Load	≤10%	≤20%
	Contact Power	≤50%	≤70%
	Contact Voltage (ac or dc)	≤50%	Below Supplier Rating
	Contact Surge Current	≤80%	≤80%
	Temperature below Maximum Limit	≥20 °C	≥20 °C
Crystals (incl. Oscillators)	Current	≤70%	Follow Manufacturer's Spec
	Drive Level Power	≤33%	Follow Manufacturer's Spec
	Voltage	Follow Manufacturer's Spec	Follow Manufacturer's Spec
	Temperature below Maximum Limit	≥30 °C	Follow Manufacturer's Spec
Opto-Isolators	Peak Voltage	≤75%	≤75%
	Current	≤70%	≤70%
	Power	≤80%	≤80%
	Junction Temperature	≤0.75 (T_j maximum - 25 °C) + 20 °C	≤0.75 (T_j maximum - 25 °C) + 20 °C
	CTR	≤75%	≤75%
Fiber Cable	Isolation Voltage	≤80%	≤80%
	Bend Radius (% Minimum Rating)	≥200%	≥200%
	Cable Tension (% Rated Strength)	≤50%	≤50%
	Fiber Tension (% Proof Test)	≤20%	≤20%
Coax Cable	Bend Radius (% Minimum Rating)	≥110%	≥110%
Printed Wiring (Circuit) Board	Absolute Maximum Temperature	10 °C less than UL rating specification of the laminate materials	UL rating specification of the laminate materials
	Solder Limit Temperature	Time at temperature exposure per UL796	Time at temperature exposure per UL796
	Minimum Creepage and Clearance	See Section 4 and Figure 4-3	See Section 4 and Figure 4-3

1. Stress Factor is the applied level divided by rating: a 12 volt rated part used at 9 volts has a 75% stress factor.
2. Components with certified safety agency approvals may be used up to 100% of their approved ratings.