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Design Guide for the Packaging of High Speed Electronic Circuits

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2215 Sanders Road, Northbrook, IL 60062-6135
Tel. 847.509.9700 Fax 847.509.9798
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Design Guide for the Packaging of High Speed Electronic Circuits

Developed by the IPC-2251 Task Group (D-21a) of the High Speed/ High Frequency Committee (D-20) of IPC

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Contact:

IPC
2215 Sanders Road
Northbrook, Illinois
60062-6135
Tel 847 509.9700
Fax 847 509.9798

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High Speed/High Frequency Committee

Chair
Thomas Bresnan
R&D Circuits

IPC-2251 Task Group

Chair
Byron Case
L-3 Communications

Technical Liaisons of the IPC Board of Directors

Nilesh S. Naik
Eagle Circuits Inc.

Sammy Yi
Flextronics International

IPC-2251 Task Group

Amit Bhardwaj, Polar Instruments (AP) Pte. Ltd.

Dr. Eric Bogatin, Giga Test Labs

Robert Bremer, Litton Systems Inc.

Christine R. Coapman, Delphi Delco Electronics Systems

David J. Corbett, Defense Supply Center Columbus

Theodore Edwards, Dynaco Corp.

Werner Engelmaier, Engelmaier Associates, L.C.

Martyn Gaudion, Polar Instruments Limited

Michael R. Green, Lockheed Martin Space Systems Company

Richard P. Hartley, C.I.D., Hartley Enterprises

Phillip E. Hinton, Hinton ‘PWB’ Engineering

David H. Hoover, Multek

Michael Jouppi, Thermal Man, Inc.

Thomas E. Kemp Rockwell Collins

George T. Kotecki, Northrop Grumman Corporation

Rene R. Martinez, Northrop Grumman

Deepak K. Pai, C.I.D.+, General Dynamics-Advanced Information

Nicholas G. Paulter, NIST

Mohammad Rahnavard, Xerox Corporation

John Reynolds, Rogers Corporation

Lowell Sherman, Defense Supply Center Columbus

Ken Taylor, Polar Instruments, Inc.

Daniel Welch, Arlon MED

Philip R. Wellington, L-3 Communications

Shlomi Zigdon, B.Sc., C.I.D., Shlomi Zigdon Technologies Ltd.

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Design Guide for the Packaging of High Speed Electronic Circuits

1 GENERAL

1.1 Purpose The object of this document is to provide guidelines for the design of high-speed circuitry. The subjects presented here represent the major factors that may influence a high-speed design. This guide is intended to be used by circuit designers, packaging engineers, circuit board fabricators, and procurement personnel so that all may have a common understanding of each area.

1.2 Scope The goal in electronic packaging is to transfer a signal from one device to one or more other devices through a conductor. Considerations include electrical noise, electromagnetic interference, signal propagation time, thermo-mechanical environmental protection, and heat dissipation. High-speed designs are defined as designs in which the interconnecting properties affect circuit function and require consideration. Every electrical concept has relevant physical implementation data and limitations provided to match the electrical and mechanical relationships. This guideline presents first order approximations for each of the subject areas covered. If more detail is required, the papers presented in the bibliography may provide more detailed supplemental data. Since most high speed design requires signal intergity and EMI techniques, often field solvers, signal integrity simulation tools, EMI/EMC simulation programs may be required for resolving design challenges. Many PWB layout design tools include these tools as options to their programs. These simulators are driven by SPICE, IBIS, or other models. References to manufacturers of these tools may be found on the IPC Web site (www.ipc.org).

1.3 Symbology, Terms and Definitions

1.3.1 Symbology

Symbol	Description
ABT	Advanced Bipolar-CMOS Technology
AC	Advanced CMOS
AC	Alternating Current (Time varying current)
ACQ	Advanced CMOS Quiet
ACT	Advanced CMOS TTL Compatible
ACTQ	Advanced CMOS TTL Compatible Quiet
AGP	Advanced Graphics Port Logic
AHC	Advanced High-Speed CMOS
AHCT	Advanced High-Speed CMOS TTL Compatible
ALS	Advanced Low Power Schottky Technology
AS	Advanced Schottky Technology
BCT	Bipolar-CMOS Technology
CMOS	Complimentary Metal Oxide Semiconductor
COB	Chip-On-Board
CTE	Coefficient of Thermal Expansion
CTE_{XY}	X and Y-Axis Coefficient of Thermal Expansion
CTE_Z	Z-Axis Coefficient of thermal expansion
CTT	Center Tap Terminated Logic
DC	Direct Current
DIP	Dual In-line Package
DWB	Discrete Wiring Board
dV/dT	Delta Voltage/Delta Time (Edge Slew Rate)
ECL	Emitter Coupled Logic
EMI	Electromagnetic Interference
ESD	Electro-Static Discharge
F	Fast Bipolar Logic Technology
FR-4	Flame Retardant Level 4, Epoxy Glass Dielectric Material
GaAs	Gallium Arsenide Technology
GTL	Gunning Transceiver Logic
GTL+	Gunning Transceiver Logic Plus
HC	High-Speed CMOS Technology
HCT	High-Speed CMOS TTL Compatible
HL	High-to-Low Signal Edge Transition
HSTL	High-Speed Transceiver Logic
IBIS	I/O Buffer Information Specification
IBuf	Input Buffer
IC	Integrated Circuit
K_B	Backward Crosstalk
K_F	Forward Crosstalk
L_G	Ground Plane Inductance
L_H	Low-High Signal Edge Transition
L_P	Power Plane Inductance
LVDS	Low Voltage Differential Signalling
LVEL	Low Voltage ECL
LVPECL	Low Voltage PECL
LVCMOS	Low Voltage CMOS Technology
LVT	Low Voltage Technology

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LVTTL	Low Voltage TTL Technology
LVX	Low Voltage CMOS Translation
OBuf	Output Buffer
PCI	Peripheral Component Interconnect
PDN	Power Distribution Network
PDS	Power Distribution System
PECL	Positive ECL Technology
PWB	Printed Wiring Board
R_C	Series Lead Resistance
R_G	Ground Plane Resistance
R_P	Power Plane Resistance
RSECL	Reduced Swing ECL
R_T	Sheet Resistance
Si-Ge	Silicon-Germanium
SM	Surface Mount
SPICE	Simulation Program with Integrated Circuit Emphasis
SSTL	Stub Series Terminated Logic
TAB	Tape Automated Bonding
Tan δ	Dissipation Factor (Loss Tangent)
TDR	Time Domain Reflectometer
t_f	10%-90% Edge Transition Time (Fall Time)
t_P	Total Signal Line Propagation Delay Time
t_{PD}	Propagation Delay Per Unit Length
t_r	10%-90% Edge Transition Time (Rise Time)
TTL	Transistor Transistor Logic
Z_O	Characteristic Line Impedance (Unloaded)
Z_O'	See 5.6.4
ε_r	Real Part of Relative Permittivity
$\varepsilon_{r,eff}$	Real Part of Effective Relative Permittivity
δ	Skin Depth

1.3.2 Terms and Definitions The terms listed below are used in this document. Their definitions are given in order to help the new reader. These definitions are also found in IPC-T-50, ''Terms and Definitions for Interconnecting and Packaging Electronic Circuits.'' Where possible, definitions that appear in the body of this document are referred to as follows: ''Bus - 5.6.7.2.'' This indicates that a definition for ''Bus'' appears in 5.6.7.2, and will not be repeated here.

AC Impedance – The combination of resistance, capacitive reactance, and inductive reactance experienced by time-varying voltage.

Alternating Current (AC) – A current that varies with time. This label is commonly applied to a power source that switches polarity many times per second, such as the power supplied by utilities. An AC signal may take a sinusoidal shape, but could be a square or triangular wave shape.

Amplitude – The difference between the high level and the low level of a voltage or current signal.

Analog Ground Plane – A solid copper or electrically conductive plane or plane-shape within a layer of a PWB. It provides a low inductive Analog ground signal reference (return path) for analog signal conductors on adjacent or buried layers. It also provides ground interconnect for analog active and passive analog devices.

Asymmetrical Dual-Strip Stripline – A stripline where the signal conductor that is embedded between two ground planes is not centered between them.

Attenuation – Reduction in the amplitude of a signal due to losses in the media through which it is transmitted.

Backward Crosstalk – Noise induced into a quiet line by an adjacent active line as seen at the end of the quiet line that is closest to the signal source. Typically, backward crosstalk is an inductive form of Crosstalk.

Broadside Coupled Pair – Signal conductors on adjacent layers that are routed parallel to each other, exhibits mutual trace-width coupled impedance between them, typically 50 to 150 ohms. Usually the conductors are matched in length or delay to a given tolerance.

Bulk Decoupling Capacitor – A capacitor that provides low frequency charge storage. Typically a tantalum or aluminum electrolytic dielectric capacitor placed at the power input of a circuit board and others distributed throughout the printed wiring board to reduce noise power and provide energy storage for high frequency decoupling capacitors.

Bus – See 5.6.7.2.

Busbar – A large copper or brass bar used to carry high power supply currents onto a printed wiring board (PWB) or backplane.

Capacitance – A measure of the ability of two adjacent conductors separated by an insulator to hold a charge when a voltage is impressed between them. Measured in Farads.

Characteristic Impedance – The vector sum of the impedance and reactance of a parallel conductor structure to the flow of AC current. Usually applied to transmission lines in printed boards and to cables carrying high-speed signals. Normally the characteristic impedance is a constant value over a wide range of frequencies and typically is referred to as Z_O.

Chassis Ground Plane – An electrically conductive metal layer within a printed wiring board that provides a low inductance reference (return path) for signal conductors on adjacent or buried conductors. The chassis ground plane may also be placed on the top and bottom layers of a

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